

	C)DC level	D)all are correct	
Q.12)	A biased clipper is used to limit the _____ of a waveform at a level other than 0v.		D
	A) frequency	B) intensity	
	C)time	D)amplitude	
Q. 13)	Clamper clamps the _____ peak at the zero volt.		D
	A) Can't say	B) positive	
	C)negative	D) b&c are correct	
Q. 14)	The _____ circuit is used to introduce a DC level into an AC signal.		A
	A) clamper	B) limiter	
	C)clipper	D)all are correct	
Q. 15)	The phase in the integrator and differentiator circuit respectively are		C
	A) +90 degrees and +90 degrees	B)90 degrees and -90 degrees	
	C)-90 degrees and +90 degrees	D)90 degrees and -90 degrees	
Q. 16)	External _____ voltages are applied to bias a transistor.		A
	A) DC	B) AC	
	C)Both DC and AC	D) Analog	
Q. 17)	Transistor biasing represents conditions		B
	A) AC	B) DC	
	C)both AC and DC	D)none of the above	
Q. 18)	Operating point represents		B
	A) The magnitude of signal	B) Zero signal values of IC and VCE	
	C)Values of IC and VCE when signal is applied	D)none of the above	
Q. 19)	For faithful amplification by a transistor circuit, the value of VBE should for a silicon transistor		B
	A) Be zero Be between 0 V and 0.1 V	B) Not fall below 0.7 V	
	C)Be 0.01 V	D)Be zero	
Q. 20)	The circuit that provides the best stabilization of operating point is		A
	A) Potential divider bias	B) Base bias with emitter feedback	
	C)Collector feedback bias	D)Base resistor bias	
Q.21)	In FET the noise level is _____		C
	A) Low	B) High	
	C) Very Low	D) Moderate	
Q. 22)	A JFET is also called transistor		C
	A) Bipolar	B) Current Controlled	
	C)Unipolar	D) Bidirectional	
Q. 23)	The gate of a JFET is biased		C
	A) forward	B) reverse as well as forward	
	C)reverse	D)Connected to Vds	
Q. 24)	In a p-channel JFET, the charge carriers are		A
	A) holes	B) electrons	
	C) Both holes and electrons	D) minority charge carriers	
Q. 25)	If the reverse bias on the gate of a JFET is increased, then width of the conducting channel		C
	A) is increased	B) remains the same	
	C)is decreased	D)Becomes zero	
