D.Y. PATIL COLLEGE OF ENGINEERING & TECHNOLOGY
KASABA BAWADA KOLHAPUR-416006
(An Autonomous Institute)
S. Y. B. Tech (ETC), Sem-III

Q. Paper Code: 23SYET202302
Set-: I

END SEMESTER EXAMINATION (ESE), JAN. – 2023

Course Name: **Electronics Circuit Analysis and Design-1,** Course Code: **201ETL202**

Seat No:

Day and Date: Wednesday, 18.01.2023

Time: 2.00 am to 4.00 pm **Max. Marks- 50**

Instructions:

i. Question No. 1&2 is compulsory
ii. Figure to the right indicate full marks.
iii. Give suitable general Instructions
iv. Any other Course Specific Instructions.

BT	CO's	Q. No.		Marks
		Q.1	**All Questions are compulsory**	**20**
	CO2	**a**	Design unregulated power supply to produce 8V, 20mA with 2% ripple	**6M**
1,2	**CO1**	**b**	Draw and explain series pass voltage regulator. What is overload protection circuit used in it.	**7 M**
1,2	**CO1**	c	Design an adjustable voltage regulator using LM 317 which provides the following specifications Vo=5V to 12 V at $I_{L\ max}$ =50mA.	**7 M**
		Q.2	**All Questions are compulsory**	**10**
1,2	**CO2**	**a**	Draw and explain Negative clipper with positive bias circuit using necessary waveform. **Or** Draw the circuit diagram of integrator and derive the output equation.	**4**
1,2	**CO1**	**b**	What is positive clamper with negative bias. Draw input output waveform for pulse wave of 8V peak to peak and -3V bias	**6**
		Q.3	**All Questions are compulsory**	**10**
1,2	**CO1**	**a**	What is thermal runaway	**3**
1,2	**CO1**	**b**	Draw and explain collector to bias with its operating point equations **Or** Derive the stability factor of voltage divider Bias circuit.	**7**
		Q.4	**Attempt any two out of three questions**	**10**
1,2	**CO1**	**a**	Explain JFET with its characteristics	**5**
1,2	**CO1**	**b**	Compare BJT and JFET.	**5**
1,2	**CO1**	**C**	Explain self-bias of JFET	**5**

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