Total No. of Question : [6]

Registration No. :

Programme Name : Bachelor of Electronics and Telecommunication Engineering
Regular S.Y.B.Tech. ESE (A.Y. 2023-24) Sem. III Nov.2023
III SEMESTER (2022 BATCH)
201ETL202-Electronics Circuits Analysis and Design - I (TH)

Duration : [11:00 AM - 01:00 PM]
Date : 23 Nov, 2023
Day : Thursday

Marks : 50

Instructions :

(Q1) Design an unrgulated power supply with CTFWR and series inductor filter to produce 11V, 15mA [7.0] and ripple factor of 0.19.

      CO :- 1, 2
      Blooms Taxonomy :- Analyze

(Q2) How Emitter follower voltage regulator performs line and regulation and load regulation explain [6.0] with circut diagram.

      CO :- 1, 2
      Blooms Taxonomy :- Analyze

(Q3) Using 7812 IC regulator, design a current source which will deliver 0.25Amp current to 860 Ohm [7.0] load. Draw neat circuit daigram

      CO :- 1, 2
      Blooms Taxonomy :- Analyze

(Q4) Solve the following [10.0]

      CO :- 3
      Blooms Taxonomy :- Apply

(4.1) Draw the circuitdiagramand input, output waveform with magnitude and analysis for 10 V [4.0] input square waveform and 2V biasing voltage for negative clamper with positive bias.

OR [4.1 / 4.2]

(4.2) Draw the circuitdiagramand input, output waveform with magnitude and analysis for 8 [4.0] V input sinusoidal waveform and 3V biasing voltage for series positive clipper with positive bias.

(4.3) Draw circuit diagram and frequency response graph for High pass Filter. Prove that [6.0] HPF can be used as differentiator under certain conditions

(Q5) Solve the following [10.0]

CO :- 4
Blooms Taxonomy :- Analyze

(5.1) What are the advantages and disadvantages of fixed bias of BJT   [3.0]

(5.2) Derive the expression for Vce, Ic & stability factor (S) of C to B bias of BJT   [7.0]

OR [5.2 / 5.3]

(5.3) Determine V_{CE},$\mathbf{E}_{TH}$,$\mathbf{R}_{TH}$of self bias if R1=2.2K, R2=8.2K, Re=1K, Rc=3.3K, Vcc=12V,   [7.0]
Beta of BJT=110

(Q6) Solve any 2   [10.0]

CO :- 4
Blooms Taxonomy :- Analyze

(6.1) Explain working of JFET with Output characteristics   [5.0]

(6.2) For JFET determine Id if Vgs=1.5V, Idss=20mA, Vp=7V   [5.0]

(6.3) Explain self bias of Junction field effect Transistor   [5.0]

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