

**Day and Date: Friday, 17/06/2022**

**Time: 9.30 to 1.15**

**Max. Marks- 100**

**Instructions:**

- i. Question No. 1 is compulsory.
- ii. Figure to the right indicate full marks.
- iii. Assume suitable data wherever necessary.

BT	CO's	Q. No.		Marks
		<b>Q.1.</b>	<b>Attempt the following.</b>	<b>40</b>
3	CO1	<b>a.</b>	i) Sketch the logic symbol of 2- input XNOR gate and draw its truth table. Why it is called as coincidence detector? ii) Derive all other gates from NAND gate .	5 5
3	CO1	<b>b.</b>	Sketch & analyze the working of 8 to 1 multiplexer with the help of block diagram, logic diagram & truth table.	10
4	CO2	<b>c.</b>	i) Draw a logic symbol of S-R FLIP-FLOP with -ve edge triggered clock input & analyze its working using truth table. ii) Draw a logic symbol of T FLIP-FLOP with -ve edge triggered clock input & analyze its working using truth table.	5 5
4	CO1	<b>d.</b>	Analyze & minimize the following expression using k-map i) $Y(A,B,C)=\sum m(1,3,5,7)$ ii) $Y(A,B,C)=\sum m(0,1,4,5)$	10
		<b>Q.2.</b>	<b>Attempt the following.</b>	<b>20</b>
4	CO2	<b>a.</b>	Draw a logic diagram & timing waveform of 2-bit asynchronous up counter using J-K flipflops and analyze its working. <b>OR</b> Draw a logic diagram of 2-bit ripple up/down counter using negative edge triggered J-K flipflops and analyze its working	8
4	CO2	<b>b.</b>	Analyze mod-6 asynchronous counter using T-flipflops.	8
4	CO2	<b>c.</b>	Analyze the effect of propagation delay in ripple counters.	4
		<b>Q.3.</b>	<b>Attempt any 4 of the following sub questions.</b>	<b>20</b>
4	CO4	<b>a.</b>	Analyze the working of 4 - bit gray to binary code converter with the help of Verilog code.	5

4	CO4	<b>b.</b>	Analyze the working of negative edge triggered T flip flop with the help of Verilog code.	5
4	CO4	<b>c.</b>	Analyze the working of 4 bit binary down counter with the help of Verilog code.	5
4	CO4	<b>d.</b>	Analyze the working of 4 - bit binary to grey code converter with the help of Verilog code.	5
4	CO4	<b>e.</b>	Analyze the working of 2 to 4 decoder with the help of Verilog code.	5
<b>Q.4 Attempt the following.</b>				
2	CO3	<b>a</b>	Describe the working of R/W memory with the help of block diagram.  <b>OR</b>  Describe static RAM cell with suitable diagram.	5
2	CO3	<b>b</b>	What is PLA? Describe with the help of suitable diagram.	5
2	CO3	<b>c</b>	What are the basic configuration of PLDs? Draw its suitable diagrams.	5
2	CO3	<b>d</b>	Compare between CPLD & FPGA.	5

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