

Total No. of Question : [4]

Registration No. :

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Programme Name : Bachelor of Electronics and Telecommunication Engineering
Regular S.Y.B.Tech.Sem.IV ESE May / June 2023
IV SEMESTER (2021 BATCH)
201ETL212-Digital System Design using Verilog

Duration : 2 Hours

Marks : 50

Instructions :

(Q1) All Questions are compulsory [20.0]

(1.1) Solve the following Boolean expression using Quine -Mc Cluskey method. [8.0]
 $F(A,B,C,D) = \text{Summation } m(1,2,3,7,8,9,10,11,14,15)$

CO :- 1

Blooms Taxonomy :- Analyze

(1.2) Design & implement full subtractor by constructing the truth table and simplifying the output equations [6.0]

CO :- 2

Blooms Taxonomy :- Create

(1.3) Convert an SR Flip-Flop into D Flip-Flop. [6.0]

CO :- 2

Blooms Taxonomy :- Create

(Q2) All Questions are compulsory [10.0]

(2.1) Design a Mod 6 synchronous counter using D flip-flop [7.0]

CO :- 2

Blooms Taxonomy :- Create

OR [2.1 / 2.2]

(2.2) Design 3 bit down Asynchronous(ripple) counter using T flipflop and explain with suitable waveforms [7.0]

CO :- 2

Blooms Taxonomy :- Create

(2.3) What is state diagram? Explain with suitable example [3.0]

CO :- 2

Blooms Taxonomy :- Create

(Q3) All Questions are compulsory [10.0]

(3.1) Write Verilog code for 4 to 1 Multiplexer [5.0]

CO :- 4

Blooms Taxonomy :- Create

OR [3.1 / 3.2]

(3.2) Write Verilog code for 3 to 8 decoder [5.0]

CO :- 4

Blooms Taxonomy :- Create

(3.3) Explain different types of Verilog operators [5.0]

CO :- 4

Blooms Taxonomy :- Create

(Q4) Attempt any two out of three questions [10.0]

(4.1) Implement full adder using ROM. [5.0]

CO :- 3

Blooms Taxonomy :- Understand

(4.2) Draw and explain static RAM . [5.0]

CO :- 3

Blooms Taxonomy :- Understand

(4.3) Distinguish between CPLD and FPGA [5.0]

CO :- 3

Blooms Taxonomy :- Understand
