SL-475

Total No. of Pages : 2

Seat No.	

B.E. (Computer Science & Engineering) (Semester-VII) (Revised) (New) Examination, May - 2017
ADVANCED COMPUTER ARCHITECTURE
Sub. Code : 67541

Day and Date : Monday, 15-05-2017 **Total Marks : 100**

Time : 2.00 p.m. to 5.00 p.m.

Instructions :
1) **Attempt any three questions from each section.**
2) **Figures to right indicate full marks.**
3) **Assume suitable data if necessary.**

SECTION-I

Q1) a) Explain with block diagram Flynn's classification of computer architectures. **[8]**

b) What is MTBF? How it is measured? **[8]**

Q2) a) Explain the concept of linear pipelining. State the factors on which throughput rate is dependent. **[8]**

b) What are systolic arrays? Draw architecture of systolic array. How systolic arrays are different than SIMD array processors? **[8]**

Q3) a) Draw and explain scalable coherent multiprocessor model with distributed shared memory. **[8]**

b) What are different characteristics of the Cray-1 computer system. With block diagram explain front end system interface with Cray-1 architecture. **[8]**

Q4) Write Short Notes on (Any Three). **[3×6=18]**

a) Principle of multithreading

b) Associative Processors

c) Illiac IV - array processor

d) Vector Instructions

P.T.O.

SECTION-II

Q5) a) What is K map in Cm* loosely coupled architecture? What is function on queues in K map? **[8]**

b) Draw and explain the basic structure of a vector architecture VMIPS. **[8]**

Q6) a) What are Bernstein's conditions? How the parallelism in the code is checked? **[8]**

b) Draw and explain GPU memory structure. **[8]**

Q7) a) What is latency? State different latency hiding techniques? Explain any one in detail. **[8]**

b) What is data dependency analysis? How it is achieved? **[8]**

Q8) Write Short Notes on (Any Three). **[3×6=18]**

a) Grain packing

b) Hardware and Software parallelism

c) Tightly coupled architectures

d) Slocal