Seat No.	

SV - 193

Total No. of Pages : 2

S.E. (CSE) (Part - II) (Semester - IV) Examination, May - 2018
COMPUTER ORGANIZATION
Sub. Code: 63533

Day and Date : Friday, 11 - 05 - 2018
Time : 9.30 a.m. to 11.30 a.m.

Total Marks : 50

Instructions :
1) **Solve all questions.**
2) **Q. No. 1 and Q. No. 4 is compulsory.**
3) **Solve any one from Q. No. 2, 3 and one from Q. No. 5, 6.**
4) **Figures to right indicate full marks.**

Q1) a) Write the IEEE 754 32 bit floating point number format. **[1]**

b) Illustrate Booth multiplication algorithm for X = 10110011 Y = 11010101. **[6]**

c) Write Non-restoring division algorithm for unsigned integres. **[6]**

Q2) a) Explain basic features of third generation computer. **[6]**

b) Explain VLSI era. **[6]**

Q3) a) Write HDL format for Z = X + Y using single address instruction. **[6]**

b) Explain a typical CPU with general register organization. **[6]**

Q4) a) Explain structure of a Set-associative memory. **[6]**

b) Explain all page replacement policies for the paging system in which M1 has a capacity of 3 pages. The execution of a program Q requires reference to five distinct pages Pi, i < = 5 and i is page address. The page address stream formed by executing Q is

2 3 2 1 5 2 4 5 3 2 5 2 **[6]**

P.T.O.

Q5) a) Explain with architecture diagram P-IV processor. [6]

b) Explain Wilkes basic structure of a micro programmed control unit. [6]

Q6) a) Design GCD processor using classical method. [6]

b) Draw and explain a neat diagram of twos complement multiplier with a set of control points. [6]

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