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S.E. (Electronics) (Semester - III)(Revised) Examination, November - 2018

ENGINEERING MATHEMATICS - III

Sub. Code : 63434

Day and Date : Tuesday, 20- 11 - 2018 **Total Marks : 100**

Time : 10.00 a.m. to 01.00 p.m.

Instructions: 1) **All questions are compulsory.**
2) **Figures to the right indicate full marks.**
3) **Use of non programmable calculator is allowed.**

SECTION - I

Q1) Solve any three **[18]**

a) Solve $(D^3 - 2D^2 - 5D + 6)y = \cosh 2x$

b) Solve $(D^2 - 2D + 4)y = 3x^2 - 5x + 2$

c) Solve $(D^2 - 2D + 2)y = e^x \sin x$

d) A condenser of capacity C is discharged through the inductance L and a resistance R in series and the charge q at any time t satisfies the equation

$$L\frac{d^2q}{dt^2} + R\frac{dq}{dt} + \frac{q}{c} = 0$$

Given that L = 0.25 henry. R = 250 ohms

$C = 2 \times 10^{-6}$ farads. When t = 0, the charge q is 0.002 coulombs and the current $\frac{dq}{dt} = 0$. Obtain the value of q in terms of t.

Q2) Solve any two **[16]**

a) Find the directional derivative of $\phi = x^2 + 2y^2 - 3z^2$ at (1,2,1) in the direction.

i) Normal to $xy^2 + yz^3 = 4$ at (1,–1,1)

ii) Tangent to $x = t^2 + t$, $y = 2t$, $z = 2 - t$ at t = 1.

b) Show that $\bar{F} = (z^2 + 2x + 3y)i + (3x + 2y + z)j + (y + 2xz)k$ is irrotational but not solenoidal and hence find scalar potential

c) Prove that $\nabla \cdot \left[r \nabla \left(\frac{1}{r^3} \right) \right] = \frac{3}{r^4}$

P.T.O.

Q3) Solve any two **[16]**

a) A random variable has probability distribution function

$$f(x) = \frac{1}{k} \cdot \frac{1}{1+x^2}, -\infty \le x \le \infty$$

i) Determine k

ii) Find P($0 \le x \le \infty$)

b) If the probability that an individual suffers a bad reaction from a certain injection is 0.001. Determine the probability that out of 2000 individuals

i) exactly 3

ii) more than 2 individuals

iii) none

iv) more than one individual will suffer a bad reaction

c) The customer accounts of a certain departmental store have an average balance of Rs. 120 and standard deviation of Rs.40. Assuming the distribution of account balance is normal find the proportion of accounts

i) over Rs. 150

ii) between Rs.100 and Rs.150

iii) between Rs. 60 and Rs.90

iv) below Rs.60

[Given : For S.N.V.Z, the area from z=0 to z=0.75 is 0.2734, the area from z=0 to z=0.5 is 0.1916, the area from z=0 to z=1.5 is 0.4332]

SECTION - II

Q4) Attempt any three from the following:

a) Find Laplace transform of **[6]**

$$f(t) = t/a, \ 0 < t \le a$$

$$= \frac{1}{a}(2a - t), \ a < t < 2a$$

and $f(t + 2a) = f(t)$

b) Find inverse laplace transform of $\frac{1}{s(s+1)(s+2)(s+3)}$ **[6]**

c) Given f(t) = t + 1, $0 \le t \le 2$ **[6]**

= 3 , t >2

Find $L[f(t)]$ and $L[f'(t)]$?

d) Solve using Laplace transform **[6]**

$\frac{d^3y}{dt^3} + 2\frac{d^2y}{dt^2} - \frac{dy}{dt} - 2y = 0$ where y(0) =1, y'(0) = 2 and y''(0) = 2.

Q5) Attempt any two of the following :

a) Obtain the fourier series for the function $f(x)$ given by **[8]**

$f(x) = x + \frac{\pi}{2}, \quad -\pi \le x \le 0$

$= \pi/2 - x, \quad 0 \le x \le \pi$

and hence deduce that $\frac{1}{1^2} + \frac{1}{3^2} + \frac{1}{5^2} + --- \infty = \frac{\pi^2}{8}$.

b) Expand the function $f(x) = x - x^2$ as a fourier series in the interval $-1 \le x \le 1$. Hence show that $\frac{1}{1^2} - \frac{1}{2^2} + \frac{1}{3^2} - \frac{1}{4^2} + --- \infty = \frac{\pi^2}{12}$. **[8]**

c) If f(x) = 0, $-\pi \le x \le 0$ **[8]**

= sin$x$, $0 \le x \le \pi$

Prove that $f(x) = \frac{1}{\pi} + \frac{1}{2}\sin x - \frac{2}{\pi}\sum_{n=1}^{\infty} \frac{\cos 2nx}{4n^2 - 1}$

Hence show that i) $\frac{1}{1.3} + \frac{1}{3.5} + \frac{1}{5.7} + --- \infty = \pi/2$

ii) $\frac{1}{1.3} - \frac{1}{3.5} + \frac{1}{5.7} + --- \infty = \frac{\pi - 2}{4}$

Q6) Attempt any two of the following : **[8]**

a) Find fourier transform of the function

$f(x) = 1-x^2, \quad |x| \leq 1$

$= 0, \quad |x| > 1$

and hence evaluate $\int_0^\infty \left(\frac{x\cos x - \sin x}{x^3}\right)\cos\left(\frac{x}{2}\right)dx.$

b) Find the fourier sine and cosine transform of the following function **[8]**

$f(x), = x, \quad 0 \leq x \leq 1$

$= 2 - x, \quad 1 \leq x \leq 2$

$= 0, \quad x > 2$

c) Using inverse fourier sine transform find $f(x)$, if $F_s(s) = \frac{1}{s}e^{-as}$ **[8]**

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S.E. (Electronics) (Semester - III) (Revised) Examination, November - 2018

ELECTRONIC MEASUREMENT AND INSTRUMENTATION

Sub. Code : 63435

Day and Date : Saturday, 24- 11 - 2018 **Total Marks : 100**

Time : 10.00 a.m. to 01.00 p.m.

Instructions: **1)** **All questions are compulsory.**

2) **Figures to the right indicate full marks.**

SECTION - I

Q1) Attempt any two of the following: **[16]**

a) Draw block diagram of measuring system and explain each block in detail.

b) Explain the principle of operation of ohm-meter.

c) Explain with the help of neat block diagram the working of Vertical Deflection System of CRO.

Q2) Attempt any two of the following: **[16]**

a) What is logic analyzer? Explain the operation of logic analyzer with neat block diagram. State its applications.

b) Draw and explain pulse and square wave generator.

c) Explain the static and dynamic characteristics of a instrument.

Q3) Write short note on any three of the following: **[18]**

a) Digital Multimeter.

b) Dual beam oscilloscope.

c) Signal Generators.

d) Fourier analyzer.

P.T.O.

SECTION - II

Q4) Attempt any two of the following **[16]**

a) What is Strain Gauge? Derive expression for Gauge Factor.

b) Derive Bridge Balance condition for wien Bridge.

c) Explain in detail binary weighted DAC.

Q5) Attempt any two of the following : **[16]**

a) Explain piezoelectric transducer in detail.

b) A Maxwells Bridge is used to measure inductive impedance Bridge constants for balance are C1 = 0.01mf R1 = 470K R2 = 5.1K R3=100K. Find series equivalent of unknown impedance.

c) Explain block diagram of typical DAS.

Q6) Write short notes on (any three) **[18]**

a) Thermistor

b) Signal conditioning

c) Sample and hold circuit

d) Capacitive transducer

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Total No. of Pages : 2

S.E. (Electronics Engg.) (Part - II) (Semester - III) (Revised) Examination, November - 2018

ELECTRONIC CIRCUIT ANALYSIS AND DESIGN - I

Sub. Code : 63436

Day and Date : Tuesday, 27 - 11 - 2018 **Total Marks : 100**

Time : 10.00 a.m. to 01.00 p.m.

Instructions :
1) **All questions are compulsory.**
2) **Figures to the right indicates full marks.**
3) **Assume suitable data if necessary.**
4) **Standard Data sheet is allowed.**

SECTION - I

Q1) Attempt any three of the following. **[18]**

a) Explain "C" filter using full wave rectifier. Draw necessary waveforms.

b) Draw and explain different biased diode clipper circuits.

c) For a zener shunt regulator if Vz = 10V, Rs = 1KΩ, R_L = 2KΩ and input voltage varies from 20V to 40V, Find the maximum and minimum values of zener current.

d) Sketch & explain the output of high pass filter to square ware input for the following conditions.
   i) RC>>T
   ii) RC<<T

Q2) Attempt any two of the following. **[16]**

a) Design a transistorized series pass voltage regulator for the following specifications, Vi = 20 ± 20%, Vo = 12V, I_L = 1A, Sv < 0.03.

b) A 250 – 0 – 250 Vrms transformer is used with full wave center tapped rectifier with each diode having an internal resistance of 25Ω. If the load resistance is 1KΩ. find,
   i) DC Load Current.
   ii) DC Load Voltage.
   iii) rms value of Ripple Voltage.
   iv) Rectification Efficiency.

c) Write a note on Voltage Doubler and Voltage Tripler Circuit.

P.T.O.

Q3) Attempt any two of the following. **[16]**

a) Compare rectifiers based on, No. of Diodes used, Type of Transformer, PIV, output frequency, ripple factor, efficiency, form factor, and Peak factor.

b) Design a voltage regulator using IC 723 for variable output voltage of 5 to 10V at 500mA load current from unregulated supply of 12V.

c) A 40 volt symmetrical square wave having a period of 50μS is applied as input to the RC differentiator having time constant of 5mS. Sketch the output.

SECTION - II

Q4) Attempt any three of the following. **[18]**

a) What is "Thermal Runaway"? How to avoid Thermal Runaway?

b) Draw h-parameter model for common emitter amplifier and derive equations for all h parameters.

c) Compare depletion type MOSFET and enhancement type MOSFET.

d) Derive the expression for stability factor 'S' of a fixed bias circuit.

Q5) Attempt any two of the following. **[16]**

a) Design self bias Circuit with $H_{fe} = 110$, $V_{cc} = 14V$, $V_{CEQ} = 6V$, $I_{CQ} = 5mA$.

b) Draw and explain in detail low and high frequency step response of RC coupled amplifier.

c) Design a single stage RC coupled amplifier to give output of 10 V_{PP} across the load of 2KΩ. The frequency range of operation is 30 Hz to 15 KHz. The source resistance is 600Ω. Stability factor is 10.

Q6) Attempt any two of the following. **[16]**

a) What are h parameters? Determine h parameters using characteristics of BJT connected in CE mode.

b) Draw diagram of common source FET amplifier. Derive an expression for its voltage gain at low frequency.

c) The source and load resistance connected to a BJT amplifier in CE configuration are 650Ω and 1.1KΩ respectively.
hie = 1.1KΩ, hre = 2×10^{-4}, hfe = 500, hoe = 20 μ moh.
Calculate :

i) Ai ii) Ri

iii) Av iv) Ro

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S.E. (Electronics) (Semester - III) Examination, November- 2018

ANALOG COMMUNICATION

Sub. Code : 63437

Day and Date : Thursday, 29 - 11 - 2018 **Total Marks : 100**

Time : 10.00 a.m. to 01.00 p.m.

Instructions : **1)** **All questions are compulsory.**

2) **Figures to right indicate full mark**

SECTION - I

Q1) Solve any three: **[18]**

a) Draw and explain block of analog communication system.

b) Draw and explain block diagram of TRF receiver.

c) Explain the following terms in FM

i) Frequency deviation

ii) Modulation index

iii) % Modulation

d) Comment on superhetrodyne tracking? Explain three-point tracking.

e) A carrier, amplitude modulated to a depth of 50% by a sinusoid, produces side frequencies of 5.005 MHz and 4.995 MHz the amplitude of each side frequency is 40 V. Find the frequency and amplitude of carrier signal.

Q2) Solve any Two: **[16]**

a) Draw and explain DSBSC technique with frequency spectrum of DSBSC wave.

b) Draw and explain in detail practical diode detector circuit.

c) In an FM system, when the audio frequency(AF) is 500 Hz, and the AF voltage is 2.4 V, the deviation is 4.8 KHz. If the AF voltage is now increased to 7.2V, what is the new deviation? Find the modulation index in each case.

P.T.O.

Q3) Solve any two : **[16]**

a) Explain generation of SSB signal using third method.

b) Draw block diagram of tuner used in superhetrodyne receiver and explain how constant IF output is obtained for each station.

c) If all AM broadcasting stations handle audio frequencies of up to 5 KHz, how many radio broadcasting stations can be accommodated from 1 MHz to 1.5 MHz of the medium-wave band?

SECTION - II

Q4) Solve any three : **[18]**

a) What is amplitude limiting in FM demodulation? Explain operation of amplitude limiter.

b) Draw and explain PAM modulator circuit using emitter follower with waveforms.

c) If the resistor is operating at 27°C and the bandwidth of interest is 2 MHz, then what is the maximum noise power output of resistor?

d) Define sampling theorem? Explain different types of sampling techniques used in PAM?

e) What are the various types of antenna? Explain basic radiation mechanism principle of antenna.

Q5) Solve any two : **[16]**

a) What are the types of FM demodulation? Explain slope detector curve.

b) What are various types of PTM? Explain with waveforms generation of PTM signals using direct method.

c) What is space wave propagation? Explain.

Q6) Solve any two **:** **[16]**

a) Compare AM and FM technique.

b) Explain with block diagram Flat top demodulation methods of PAM signals?

c) Explain in brief the following terms:

i) Antenna gain ii) Input impedance

iii) Beamwidth iv) Bandwidth

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S.E. (Electronics) (Semester - III) (Revised) Examination, December - 2018

NETWORK ANALYSIS

Sub. Code : 63438

Day and Date : Saturday, 01 - 12 - 2018 **Total Marks : 100**

Time : 10.00 a.m. to 01.00 p.m.

Instructions :
1) **All questions are compulsory.**
2) **Assume suitable data wherever required.**
3) **Figures to the right indicate full marks.**
4) **Use of scientific calculator is allowed.**

SECTION - I

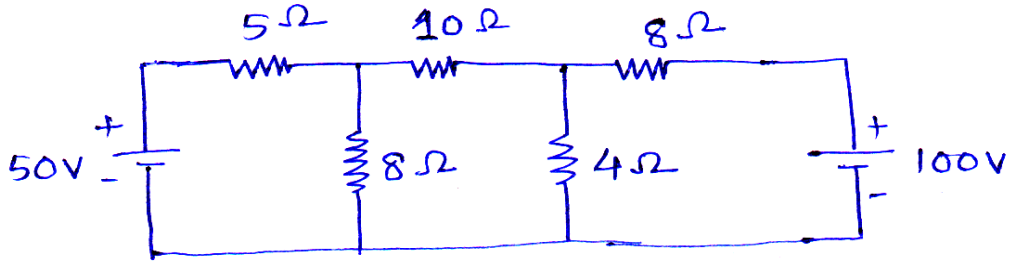
Q1) Solve any THREE. **[3 × 6 = 18]**

a) Explain following terms with suitable example.

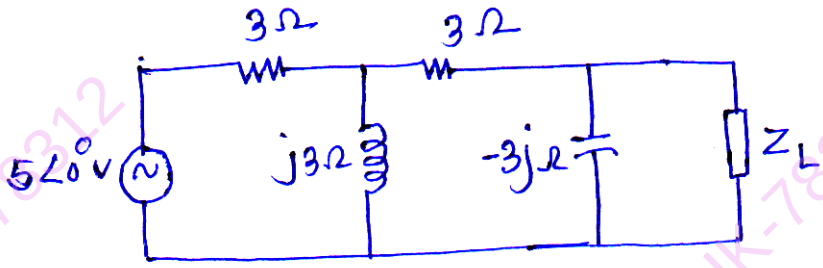
i) Incident node ii) Twings and links

iii) Tree and co-tree

b) Find current through 10 Ω resistor by the principle of superposition theorem.

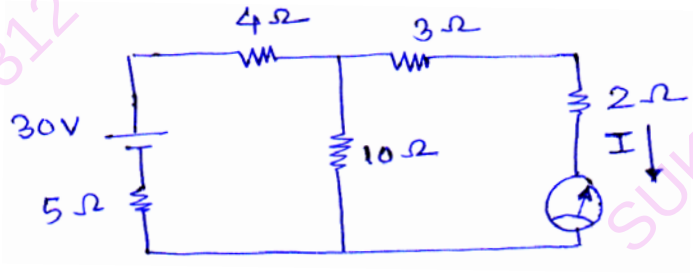


c) State and explain maximum power transfer theorem for ac networks. Find the load impedance Z_L so that maximum power can be transferred to it.



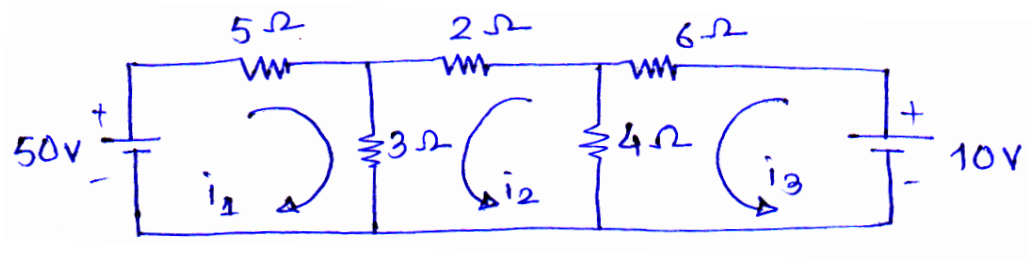
P.T.O.

d) Verify reciprocity theorem with the source and an ammeter for following network.

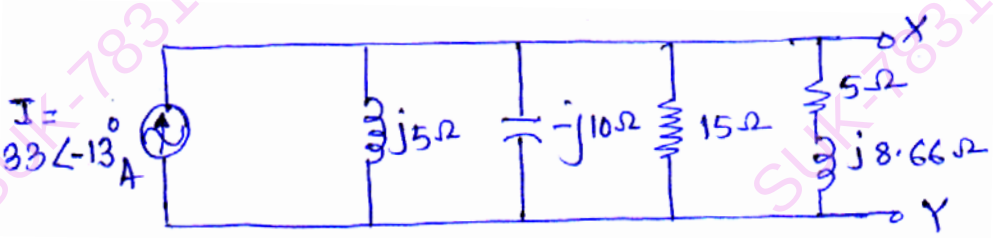


Q2) Solve any TWO. **[2 × 8 = 16]**

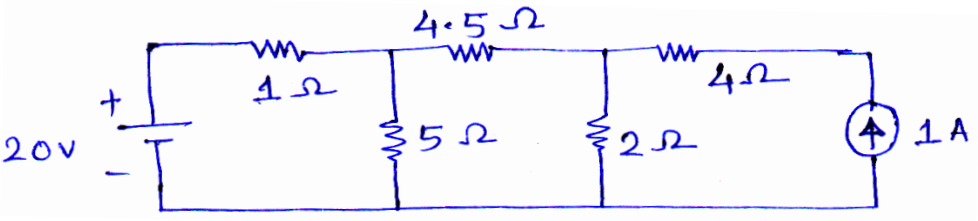
a) Determine power dissipation in 4Ω resistor of the circuit by using Mesh analysis.



b) Find Thevenin's equivalent circuit between terminals X and Y.



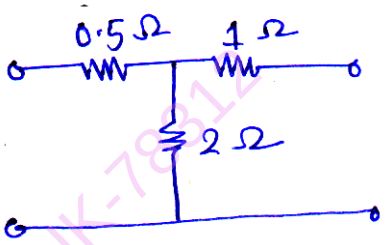
c) Use Nodal analysis method to find currents in all branches of the circuit given below.

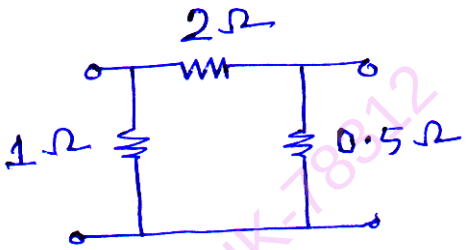


Q3) Solve any TWO. **[2 × 8 = 16]**

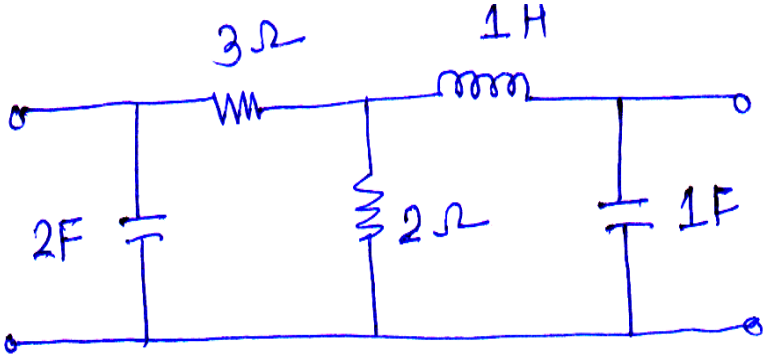
a) Express Z-parameters in terms of ABCD parameters and h-parameters.

b) Sketch the parallel-parallel connection of the given two port networks. Also find the overall Y-parameters of the resultant network.





c) Find short circuit admittance parameters for the given circuit.

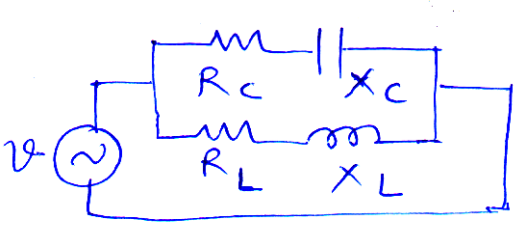


SECTION - II

Q4) Solve any Two Sub questions. **[16]**

a) Evaluate Resonance frequency of a series R-L-C circuit if R = 10 Ω, L = 2 mH, C = 10 µf. Find out Quality factor Q and Bandwidth of the circuit.

b) Derive Anti resonance frequency of a parallel circuit as shown in Figure 1 below.



c) Derive the equations for Bandwidth, Lower cut off frequency and Upper cut off frequency of R-L-C series resonance circuit.

Q5) Solve any Two Sub questions. **[16]**

a) Write short note on the restrictions of the Driving Point Functions.

b) Draw Pole- Zero map of the transfer function $G(S) = 10*(S+2)/S(S+4)(S^2+5)$

c) Define network function N(S)in terms of poles and zeros. Define the terms $Z_{11}(S)$, $G_{21}(S)$, $Z_{22}(S)$ for network function N(S).

Q6) Solve any Two Sub questions. **[18]**

a) Design a Constant k Low Pass Filter both T and π sections with cut off frequency 5 KHz and load resistance 500 Ω.

b) Design a m- derived High Pass Filter only T section with m = 0.6, cut off frequency 5 KHz and load resistance 500 Ω.

c) Design a Lattice type attenuator with 40dB attenuation and Load resistance 600 Ω.

SE -156

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S.E. (Electronics) (Semester - IV) Examination, November - 2018
LINEAR INTEGRATED CIRCUITS
Sub. Code : 63440

Day and Date : Monday, 12- 11 - 2018 **Total Marks : 100**

Time : 10.00 a.m. to 01.00 p.m.

Instructions : **1)** **All the questions are compulsory.**
2) **Assume suitable data if necessary.**

SECTION - I

Q1) Solve any three of the following : **[3 × 6 = 18]**

a) Draw neat circuit diagram of operational amplifier. Explain function of each block.

b) Draw different configuration of differential amplifier. Explain any one of it.

c) Derive and explain virtual ground concept.

d) Explain the following terms with respect to Op-amp:
   i) Slew Rate
   ii) Input Offset Current

Q2) Solve any two of the following : **[2 × 8 = 16]**

a) Explain frequency response of op-amp in open loop and closed loop configuration.

b) Explain what is circuit stability and mention different methods to test circuit stability

c) Derive closed loop voltage gain for Inverting amplifier with feedback.

Q3) Solve any two of the following : **[2 × 8 = 16]**

a) Derive and explain AC Analysis of Dual Input Balanced Output Configuration differential Amplifier.

b) Why open loop op-amp is not suitable for linear application.

c) With neat circuit diagram explain offset null techniques for op-amp configurations.

SECTION-II

Q4) Solve any three of the following : **[3 × 6 = 18]**

a) Draw and explain Window Detector.

b) With neat circuit diagram scaling and averaging amplifier.

c) Draw and explain Sample and Hold circuit.

d) Draw and explain zero crossing detector.

P.T.O.

Q5) Solve any two of the following : **[2 × 8 = 16]**

a) With help of neat circuit diagram explain the operation of Wein Bridge oscillator. Derive an expression for output frequency.

b) Write a short note on IC-566.

c) What is All pass filter? Explain its operation and draw its frequency response.

Q6) Solve any two of the following : **[2 × 8 = 16]**

a) With the help of neat circuit diagram explain V-F Converter.

b) Derive and explain Log Amplifier.

c) How will you generate square wave by using op-amp. Explain it in detail with neat circuit diagram & waveform.

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S.E. (Electronics Engg.) (Semester - IV) (Revised) Examination, November - 2018

ELECTRONICS CIRCUIT ANALYSIS AND DESIGN - II

Sub. Code : 63441

Day and Date : Tuesday, 13 - 11 - 2018 **Total Marks : 100**

Time : 10.00 a.m. to 01.00 p.m.

Instructions :
1) **All questions are compulsory.**
2) **Figures to the right indicate full marks.**
3) **Assume suitable data if necessary.**
4) **Standard Data sheet is allowed.**

SECTION-I

Q1) **Attempt any three of the following.** **[18]**

a) Prove that for class A transformer coupled power amplifier, the maximum conversion efficiency is 50%.

b) What is Negative Feedback? Discuss the effect of Negative feedback on different parameters of Amplifier.

c) Give the comparison between the different types of power amplifier based on Conduction angle, Position of Q point, Efficiency.

d) An amplifier has mid frequency gain of 100 and a bandwidth of 200 KHz.

i) What will be the new bandwidth and gain if 5% feedback is introduced?

ii) What should be the amount of negative feedback if the bandwidth is to be restricted to 1 MHz?

Q2) **Attempt any two of the following.** **[16]**

a) Design a bootstrapped emitter follower circuit to provide the following specifications:

Input impedance (Ri) = 470 KΩ, Lower 3dB frequency = 50 Hz, Vo= 3Vpp, Load resistance RL= 4.7KΩ, Source Resistance (Rs) = 620Ω.

b) Design a two stage RC coupled amplifier to meet the following specifications:

i) Load resistance (RL) = 3KΩ

ii) Source Resistance (Rs) = 460Ω

iii) Supply Voltage (V_{cc}) =12V

iv) Peak to peak output Voltage (Vopp) = 10V

v) Lower 3dB frequency (F) = 50 Hz.

c) Design transformer coupled class A power amplifier to deliver as power 2W to a load resistance of 4Ω. The transformer efficiency (η) is 70%. Use VCC 12V. Use transistor data: PD_{max} = 11W, VCE = 45V, ICMAX = 3A, hfemin = 40.

Q3) **Attempt any two of the following.** **[16]**

a) Design a two stage voltage series feedback amplifier with a overall gain of 100 and lower 3dB frequency range is 20Hz. The output voltage swing should be 12V (PP) with a load Resistance of 6KΩ. Consider Rs = 450Ω.

b) i) A sinusoidal signal Vi = 2sin 300t is applied to a power amplifier. The resulting output current is given by, Ic 15sin 300t + 1.5 sin 699t + 1.2 sin 900t = 0.5 sin 1200t

Calculate:

I) Total Harmonic Distortion (THD)

II) % increase in ac power due to distortion.

ii) Draw and explain Transformer Coupled Amplifier with frequency response.

c) Design a two stage direct coupled amplifier with the transistor specification as:

Parameter	Transistor Q1	Transistor Q2
β(min)	100	100
Icmax	100mA	100mA
VCEMAX	40v	40v
Circuit Parameters are		
VOPP	--	4V
RL	--	10KΩ
Stability Factor	5	5
%ΔICQ allowed	5%	5%
F o	20Hz	20Hz
VCC	20V	20V

SECTION-II

Q4) **Attempt any three of the following.** **[18]**

a) Draw a neat circuit of Wein Bridge Oscillator. Derive an expression for frequency of oscillation (f) and minimum gain required for sustained oscillation.

b) With a neat circuit, explain the operation of step up switch mode power supply with suitable waveforms.

c) Draw a neat circuit diagram of Schmitt trigger. Derive an expression for UTP and LTP.

d) Derive an expression for frequency of oscillation & minimum gain required for sustained oscillation in Colpitts oscillator.

Q5) **Attempt any two of the following.** **[16]**

a) Draw a neat circuit diagram of astable multivibrator. Explain its operation with waveforms at the base and collector. Derive expression for frequency of Oscillation.

b) Design a transistorized Hartley Oscillator for the following specification: Output Voltage Vo=3 V_{rms}, Frequency (f) = 10 MHz, Av = 25 Use transistor BC 147 with PD_{max} = 250mW, VCE = 45V, IC_{max} = 200mA, hfe = 330, hie = 4.5KΩ.

c) The fixed bias bistable multivibrator uses following parameters:

Vcc = 12V, –VBB = –8V, R1 = 10KΩ, R2 = 50KΩ, RC= 2.2KΩ, and hfe = 30. Calculate stable state currents and voltages for VCE (Sat)=0.2V and V BE (Sat) =0.7V.

Q6) **Attempt any two of the following.** **[16]**

a) Design a monostable multivibrator for the following specification:

Frequency F = 5 KHz, VCC = 10V, –V BB = –5V, V CE (Sat) = 0.3V, V BE (SAT) = 0.6V, Design of Trigger circuit is expected.

b) i) Write short note on Switching Regulator IC "LM 3524".

ii) Write a short note on: Crystal Oscillator

c) Design an RC phase advancing phase shift Oscillator using BJT for the following specification:

Peak to Peak Output amplitude = 5V, Frequency of Oscillation (f) = 2KHz, Use V_{cc} = 12V.

SE - 158

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Total No. of Pages : 2

S.E. (Electronics Engg.) (Part - II) (Semester - IV)
Examination, November - 2018
DATA STRUCTURES & ALGORITHMS
Sub. Code : 63442

Day and Date : Wednesday, 14 - 11 - 2018 **Total Marks : 100**

Time : 10.00 a.m. to 01.00 p.m.

Instructions : **1)** **Assume suitable data wherever necessary.**
2) **Figures to the right indicate full marks.**

SECTION - I

Q1) Answer Any 3 of the following. **[18]**

a) What is linked list? Explain its various types.

b) What is stack? Explain array representation of stack.

c) What is record? Explain record structures.

d) Describe the applications of queues.

e) Write algorithm for deletion of element from array.

Q2) Answer Any 2 of the following. **[16]**

a) Write algorithm for insertion of an element in array.

b) Write algorithm for linear search.

c) Explain queue as an abstract data type.

Q3) Answer Any 2 of the following. **[16]**

a) What is header linked list? Explain with suitable diagram.

b) Write algorithm for deletion of an element from a linked list.

c) Write algorithms for PUSH & POP operation in a stack.

P.T.O.

SECTION - II

Q4) Solve Any Two. **[16]**

a) Explain the algorithm of in order traversal of binary tree with example.

b) Define Binary tree.Explain linked representation of Binary tree with suitable diagram.

c) Explain BFS algorithm with example.

Q5) Solve Any Two. **[16]**

a) Explain construction of a heap tree. Write algorithm for insertion into the heap tree.

b) Explain shortest path algorithm with example.

c) What is hashing? Explain different hash functions.

Q6) Write short note on Any Three. **[18]**

a) Preorder traverse

b) Binary search Tree

c) Depth first search technique

d) Warshall's algorithm

Seat No.	

Total No. of Pages : 2

S.E. (Electronics Engineering) (Part - II) (Semester - IV) (Revised) Examination, November - 2018

DIGITAL SYSTEM AND MICROPROCESSOR

Sub. Code : 63443

Day and Date : Thursday, 15 - 11 - 2018 **Total Marks : 100**

Time : 10.00 a.m. to 01.00 p.m.

Instructions: 1) **Figures to the right indicate full marks.**
2) **Assume suitable data wherever necessary.**

SECTION - I

Q1) Solve any three **[18]**

a) Define following terms

i) Literals

ii) Min terms & Max terms

iii) Cronocal SOP & POS form

b) Explain Raee-round condition in J–K Flip-Flop.

c) Design 2 Bit Asynchronous Up-Down Counter.

d) Explain SR FlipFlop and J-K FlipFlop.

Q2) Solve any two **[16]**

a) Reduce the following expression using K Map & implement them in Universal Logic $\sum m\,(5,6,7,9,10,11,13,14,15)$

b) Explain the look-Ahed carry adder.

c) Implement following logic function using 8 × 1 Mux.

$F = A \oplus B \oplus C \oplus D$

P.T.O.

Q3) Solve any two **[16]**

a) Design MOD-5 Ripple Counter Using J-K Flip-Flop.

b) Write excitation table fro all Flip-Flips.

c) Explain Bidirectional Shift Register

SECTION - II

Q4) Answer any two of the following : **[2 × 8 = 16]**

a) Draw and Explain Pin out diagram of 8085.

b) Explain addressing modes of 8085 with example.

c) Compare polling, interrupt and DMA data transfer techniques in 8085 Based system.

Q5) Answer any two of the following : **[2 × 8 = 16]**

a) Draw and Explain Machine Cycle of instruction LDA 2000H.

b) State difference between memory mapped I/O and I/O mapped I/O.

c) What happens when HALT instruction is executed in 8085? Explain with state diagram

Q6) Write short notes on any three of the following **[3 × 6 = 18]**

a) CALL and RET instructions.

b) Mode 1 of 8255

c) Interrupt structure of 8085

d) 8085 Architecture

Seat No.	

Total No. of Pages : 2

S.E. (Eletronics Engineering) (Semester - IV) Examination, November - 2018

CONTROL SYSTEM ENGINEERING

Sub. Code : 63444

Day and Date : Friday, 16 - 11 - 2018 **Total Marks : 100**

Time : 10.00 a.m. to 01.00 p.m.

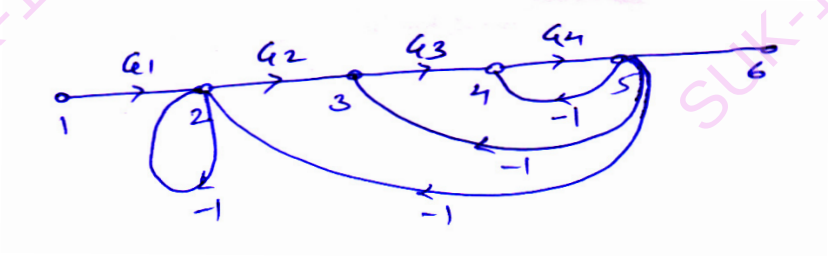
Instructions :
1) **All questions are compulsory.**
2) **Figures to the right indicate full marks.**
3) **Assume suitable data wherever necessary.**
4) **Use of graph papers are allowed.**
5) **Use of scientific calculator is allowed.**

SECTION - I

Q1) Solve Any Two. **[16]**

a) Classify control systems and explain with two examples.

b) Find overall transfer function of following signal flow graph using Mason's gain formula.



c) Explain Routh criterion for stability. Determine the stability of the system whose characteristic equation is given by $s^5 + 2s^4 + 3s^3 + 6s^2 + 5s + 3$.

Q2) Solve Any Two. **[16]**

a) Explain Reduction of parameter variations by use of feedback.

b) The open loop transfer function of unity feedback system is given by $C(s)/R(s) = 20/(S^2 + 5S + 6)$ Determine

i) Damping ratio

ii) Peak overshoot

iii) Rise time

iv) Settling time

P.T.O.

c) Draw the time response of first order system for unit step input and expression for it.

Q3) Solve Any Two. **[18]**

a) Explain standard test signals.

b) The open loop transfer function is
G (S) = K/s (s + 3) (s + 6), Sketch the root locus of the system.

c) Define time domain specifications and derive expressions for
   i) Rise time
   ii) Peak overshoot

SECTION - II

Q4) Solve Any Two. **[16]**

a) Explain Correlation between time and frequency domain Analysis.

b) For the unity feedback system G (S) = 1/S (S + 1) (S + 2). Sketch the Bode plot Determine Gain Margin and Phase Margin.

c) Explain Nyquist Stability Criterion.

Q5) Solve Any Two. **[16]**

a) Explain controllability and observability of the system.

b) Find Transfer Function from state model

$$\begin{bmatrix} x_1 \\ x_2 \end{bmatrix} = \begin{bmatrix} -5 & -1 \\ -3 & -1 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} 2 \\ 5 \end{bmatrix} U$$

$$y = [1 \quad 2] \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} D = 0$$

c) Explain concept of state, state variable and state model.

Q6) Solve Any Three. **[18]**

a) Lag compensator

b) PID Controller

c) PLC

d) Gain Margin and Phase Margin

▽▽▽▽