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Total No. of Pages : 2

T.E. (Electronics Engg.) (Semester - VI) Examination, May - 2019

VIDEO ENGINEERING (Paper - II)

Sub. Code : 66852

Day and Date : Wednesday, 15 - 05 - 2019 **Total Marks : 100**

Time : 10.00 a.m. to 01.00 p.m.

Instructions : **1)** **All questions are compulsory.**
2) **Use suitable assumptions if required.**
3) **Draw necessary figures on right side of answer sheet.**

SECTION - I

Q1) Solve any THREE. **[18]**

a) State CCIR-B standards for video broadcasting.

b) Draw the block diagram of NTSC decoder and write function of each block.

c) With suitable diagram describe how colour difference signals are generated.

d) Why the colour information requires less bandwidth than black and white information? What is additive mixing?

e) Draw suitable diagram and explain microphone and speaker.

Q2) Solve any TWO. **[16]**

a) Explain optical recording and reproduction.

b) What is Scanning? State and explain advantages of Interlace scanning.

c) Draw and explain Composite video signal for cross hatch pattern.

Q3) Solve any TWO. **[16]**

a) What is compatibility and reverse compatibility? Explain the requirements to have system compatible.

b) Explain with suitable figures the need of VSB in video broadcasting.

c) Compare Delta gun and Trinitron picture tubes for its merit and demerits.

P.T.O.

SECTION - II

Q4) Answer any THREE sub questions. **[18]**

a) Explain the composition of D MAC packet signal in details and indicate whether these can be conveyed on cable T.V. and how?

b) Discuss the compatibility problems in HD T.V. and explain the MUSE system for digital encoding of the signals.

c) Explain how a conducting matrix is created with the liquid crystal panel to reach each cell for passing charge through it. How this result in the creation of black and white areas called gray scale?

d) With the help of suitable block diagram explain the working of the block converter.

Q5) Answer any TWO sub questions. **[16]**

a) Draw the block diagram of video processor VPU-2203 and explain digital signal processing carried out in it (ITT).

b) Draw and explain the construction of LCD panels used for television.

c) With the help of suitable diagram explain the working of the satellite T.V.

Q6) Answer any TWO sub questions. **[16]**

a) Draw the block diagram of deflection processor DPU-2553 and explain digital processing carried out in it (ITT)

b) Draw the structure of the plasma display panel (PDP) used for the television and explains its working.

c) How CCTV system is different from regular T.V. broadcast? Enumerate various applications of this system of television. Describe with suitable block diagrams various methods employed to feed /transmit video signal to different Monitors/Receivers.

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Total No. of Pages : 2

Seat No.	

T.E. (Electronics and Telecommunication) (Part-III)
(Semester - VI) Examination, May - 2019
VLSI DESIGN
Sub. Code: 66917

Day and Date : Wednesday, 15- 05 - 2019 **Total Marks : 100**

Time : 10.00 a.m. to 1.00 p.m.

Instructions :
1) **All main questions are compulsory.**
2) **Figures to the right indicate full marks.**
3) **Assume suitable data if necessary.**
4) **Draw diagrams and Truth Tables wherever necessary.**

Q1) Attempt any three of the following. **[3×6=18]**

a) List important features and capabilities of VHDL.

b) Write entity diagram, truth table and VHDL code for 4:1 Multiplexer using "case" statements.

c) Explain operators in VHDL with suitable example.

d) Write entity diagram, truth table and VHDL code for D Flip-flop with synchronous reset.

Q2) Attempt any two of the following. **[2×8=16]**

a) Draw and explain VLSI Design Flow.

b) What is Package in VHDL? With the help of proper syntax and example explain package body and package declaration.

c) Write VHDL code for full adder using all three styles of modeling.

Q3) Answer any two of the following. **[2×8=16]**

a) What are the different forms of wait statement? Explain with example.

b) Design a Mealy machine for sequence detector to detect overlapping sequence 1011. Write VHDL code for the same.

c) Explain attributes in VHDL with example.

P.T.O.

Q4) Attempt any three of the following. **[3×6=18]**

a) Briefly explain about Data Types in Verilog with examples.

b) Write entity diagram, truth table and Verilog code for 2:4 decoder.

c) Draw physical structure of MOS Transistor (MOSFET). Explain the V-I characteristics of the same.

d) Write a Verilog code for JK flipflop. Provide preset and clear inputs.

e) Write schematic and layout/stick diagram for $Y = \overline{AB + C}$.

Q5) Answer any two of the following. **[2×8=16]**

a) Derive the expression for Drain current I_D of MOSFET in.

i) Linear/Resistive region ii) Saturation region

b) Draw and explain briefly architectural block diagram of XC9500 CPLD.

c) Draw the neat circuit diagram for Configurable Logic Block (CLB) used in Spartan 3E series of Xilinx make FPGA. Explain functionality of each block used inside.

Q6) Attempt any two of the following. **[2×8=16]**

a) Explain the following methodologies for testing combinational circuits. Take an example for each.

i) Stuck-at-Fault Models ii) Path sensitization

b) With neat diagram explain the concept of Built-In-Self-Test used for testing digital ICs.

c) Write a VHDL/Verilog code for Write VHDL code for up down counter using control input up/down.

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Total No. of Pages : 2

T.E. (Electronics) (Semester - V) (Revised) Examination, May - 2019

VLSI DESIGN

Sub. Code : 66283

Day and Date : Monday, 06 - 05 - 2019 **Total Marks : 100**

Time : 02.30 p.m. to 05.30 p.m.

Instructions : **1)** **All questions are compulsory.**

2) **Figures to right indicate full marks.**

3) **Assume suitable data if required.**

Q1) Attempt any three : **[18]**

a) With a suitable example describe package and configuration in VHDL.

b) Explain relational,concatination & logical opetrators in VHDL.

c) Explain different object types in VHDL.

d) Explain IEEE std.logic values in VHDL.

Q2) Attempt any two : **[16]**

a) Write VHDL code for 8-bit comparator.

b) Write VHDL code for BCD to 7-segment decoder driver with common cathod type of display.

c) Write VHDL code for 3:8 decoder using 2:4 decoder.

Q3) Attempt any two : **[16]**

a) What meta-stability and syncronizer failure? Explain in detail.

b) Write VHDL code for 4-bit binary counter.

c) Write VHDL code for divide by ten down counter.

P.T.O.

Q4) Attempt any three : **[18]**

a) Describe general form of if- then- else and case statements.

b) Design two phase clock generator using VHDL code to generate 100KHz square wave output with i) 70% duty cycle ii) 50% duty cycle.

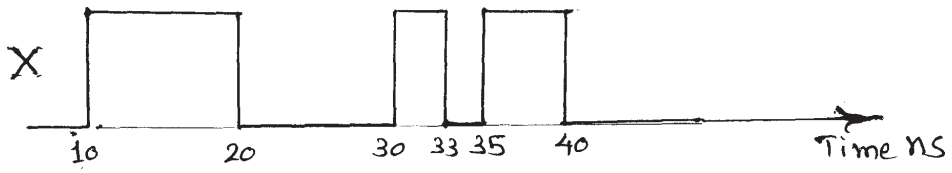
c) With a suitable example explain different types of wait statements.

d) Draw the waveforms for following statements of Z1, Z2 & Z3. Given input signal X is as showen in the waveforms.

Z1 < = transport X after 10 ns;

Z2 < = X after 10 ns;

Z3 < = reject 4 ns X after 10 ns;



Q5) Attempt any two : **[16]**

a) Describe in detail general datapath using ALU.

b) Implement the datapath for summation of n numbers.

Where n is 8-bit input no. Datapath should output the SUM. Generate the control words.

c) Draw flow chart & explain event driven simulation.

Q6) Attempt any two : **[16]**

a) Draw and explain SPARTAN-II CLB slice.

b) Explain arrangement of testing multiple circuits using BILBOs.

c) Explain with produt term allocator in CPLD.

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T.E. (Electronics Engineering) (Semester - VI) (Revised) Examination, May - 2019

POWER ELECTRONICS

Sub. Code : 66853

Day and Date : Friday, 17 - 05 - 2019 **Total Marks : 100**

Time : 10.00 a.m. to 01.00 p.m.

Instructions : **1)** **All questions are compulsory.**
2) **Figures to the right indicate full marks.**
3) **Assume suitable data if necessary.**

SECTION - I

Q1) Attempt any three of the following : **[18]**

a) Draw and explain constructional detail, working & VI characteristics of Depletion MOSFET.

b) With the help of waveform and circuit diagram explain class C commutation technique.

c) Explain why isolation is required and How it is achieved using pulse transformer.

d) Define, latching current, Holding current, forward breakover voltage, with reference to SCR.

Q2) Solve any two: **[16]**

a) Derive the equation of source current of single phase full controlled converter with RL load using Fourier analysis.

b) With the help of Block diagram and waveform explain cosine wave firing circuit for single phase bridge controlled converter.

c) Explain in detail dynamic characteristics of SCR during turn off.

P.T.O.

Q3) Attempt any two: **[16]**

a) With the help of circuit diagram explain how dv/dt and di/dt protection is achieved in SCR.

b) With the help of circuit diagram and waveform explain. How free wheeling action is inherent in single phase semiconverter with RL load. (Assume continuous current mode of operation).

c) A single phase full converter supply to resistive load. Then calculate the following performance parameter. For supply voltage of 230V firing angle $\alpha = \pi/6$, R= 10 Ω. then find out

i) Average output voltage

ii) Supply rms current

iii) Supply fundamental current

iv) Displacement factor

SECTION - II

Q4) Solve any two : **[16]**

a) Explain the operation of four-quadrant chopper.

b) State and explain control techniques of chopper.

c) A step-up chopper has an i/p voltage 200V and output voltage of 600V. If conduction time of thyristor is 200 μsec, calculate

i) chopping frequency.

ii) if pulse width is halved for operation find new output voltage.

Q5) Solve any two : **[16]**

a) Derive the following expression for single phase half-bridge voltage source inverter.

i) RMS output voltage.

ii) Instantaneous output voltage.

iii) n^{th} harmonic component

b) Explain any one harmonic reduction technique of inverter.

c) A single phase half-bridge inverter has a resistive load of 15Ω and center-tap dc i/p voltage is 96 V. Determine

i) RMS value of o/p voltage.

ii) Fundamental component of o/p voltage.

iii) Fundamental power consumed by load.

iv) RMS power consumed by load.

Q6) Solve any three : **[18]**

a) Explain switch mode AC power supply.

b) Draw and explain light dimmer using diac and triac.

c) Draw and explain operation of battery charger.

d) Block diagram of on line and off line UPs.

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T.E. (Electronics) (Semester - V) Examination, April - 2019

SIGNALS AND SYSTEMS

Sub. Code : 66280

Day and Date : Thursday, 25 - 04 - 2019 **Total Marks : 100**

Time : 02.30 p.m. to 05.30 p.m.

Instructions : **1)** **All questions are compulsory.**

2) **Figures to the right indicate full marks.**

3) **Assume necessary data, wherever required.**

SECTION - I

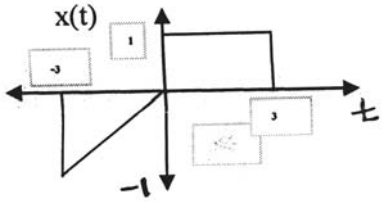
Q1) Solve any two: **[16]**

a) Identify whether the following signals are energy signal, power signal or neither of two

i) $x(t) = tu(t)$

ii) $x[n] = \left(\frac{1}{3}\right)^n .u[n]$

b) Sketch and label following



i) x(-t/2)

ii) x(t+3)

iii) x(3-t)

iv) x(t)+x(-t)

c) Find the convolution of following signals by analytical method and plot the result.

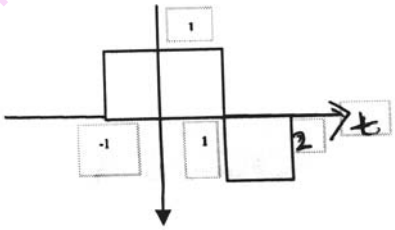
$x[n] = [1, \underset{\uparrow}{4}, 3, 2]$ and $h[n] = [\underset{\uparrow}{1}, 3, 2, 1]$

P.T.O.

Q2) Solve any two : **[16]**

a) Determine even and odd part of the following signals

i) x(t) ii) $x[n] = [1, \underset{\uparrow}{1}, 1, 1]$



b) Determine the stability and causality of following linear Time Invarient systems whose impulse responses are.

i) $h(t) = e^{-3t}\, u(t-2)$ ii) $h[n] = a^n u[n-1]$

c) State and explain convolution properties for both C, T, and D.T.

Q3) Solve any three : **[18]**

a) What is Interpolation? What are its methods? Explain band limited method.

b) Explain sampling theorem in detail.

c) Determine the Nyquist sampling rate and interval for following signals

i) $x(t) = 3\cos(1000\,\pi t) + 2\sin(2000\,\pi t)$

ii) $x(t) = (4000\,\pi t)$

d) Determine whether the following signals are periodic/aperiodic. If periodic find fundamental period.

i) $x(t) = 2\cos(3\pi t) + 7\sin(9t)$

ii) $x[n] = \cos\left(\frac{\pi}{4}n\right).\sin\left(\frac{\pi}{2}n\right)$

SECTION - II

Q4) Solve any two : **[16]**

a) Compute FT of the following and plot amplitude spectrum

$x(t) = e^{-a|t|}$ $a > 0$

b) Find the inverse ZT of the following by power series expansion method

$$X[Z] = \frac{4z}{(z^2 - 3z + 2)} \; roc\,|z| > 2$$

c) Explain the properties of DTFT.

Q5) Solve any two : **[18]**

a) Find ZT of following and determine ROC

i) $x[n] = [\underset{\uparrow}{2}, -1, 0, 3, 4]$

ii) $x[n] = [1, -2, 3, -1, \underset{\uparrow}{2}]$

b) Find the IDFT of X[K] = [4,3,2,1] and DFT of x[n] = cos(πn)

c) Explain all properties of ROC.

Q6) Solve any two : **[16]**

a) Draw the direct form II realization of following system

$y[n] = 2\,y[n-1] + 3y[n-2] + x[n] + 3x[n-1] + 2x[n-2]$

b) Draw the direct form I realization of following system represented by transferfunction $H[Z] = \dfrac{1 - z^{-1}}{1 - \frac{1}{2}z^{-1} + \frac{1z^{-2}}{4}}$.

c) With a suitable example derive general expression of linear constant coefficient differential equation of CTLTI system.

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T.E. (Electronics) (Semester - V) Examination, May - 2019
ELECTROMAGNETIC ENGINEERING
Sub. Code : 66282

Day and Date : Friday, 03 - 05 - 2019 **Total Marks : 100**

Time : 02.30 p.m. to 05.30 p.m.

Instructions :
1) **All questions are compulsory.**
2) **Figures to the right indicate full marks.**
3) **Assume suitable data if necessary.**
4) **Use of nonprogrammable calculator is allowed.**

SECTION - I

Q1) Attempt any two : **[16]**

a) Given the points P(ρ = 5, ϕ = 60°, z = 2) and Q(ρ = 2, ϕ = 110°, z = –1):
   i) Find the distance $|R_{PQ}|$;
   ii) Give a unit vector in Cartesian coordinators at P that is directed towards Q;
   iii) Give a unit vector in cylindrical coordinates at P that is directed towards Q.

b) Find the electric field intensity $\bar{E}$ at a point P due to infinite line charge distribution along the z-axis.

c) Prove the point from of ampere's law i.e. $\nabla \times \bar{H} = \bar{j}$.

Q2) Attempt any two : **[16]**

a) Given points are M(6, 2, –3), N(–2, 3, 0), and P(–4, 6,5). Find
   i) The area of the triangle they define :
   ii) A unit vector perpendicular to this triangular surface;
   iii) A unit vector bisecting the interior angle of triangle at M.

b) Find the force on a 100 μC charge at (0, 0, 3)m. If four like charges of 20 μC are located on the x and y axis at ± 4m.

c) Explain the concept of vector magnetic potential hence show that $\bar{A} = \int_{vol} \frac{\mu \bar{J} dv}{4\pi r}$.

P.T.O.

Q3) Answer any three : **[18]**

a) Find $\bar{A}+\bar{B}, \bar{A}-\bar{B}, \bar{A}.\bar{B}$ angles between $\bar{A}$ and $\bar{B}$ $\bar{A}\times\bar{B}$, unit vector normal to $\bar{A}$ and $\bar{B}$ where $\bar{A} = 5a_x + a_y + 3a_z$ and $\bar{B} = 2a_x + 2a_y + 2a_z$.

b) Find the electric charge required on the earth and moon to balance their gravitational attraction if the charge on the earth is 10time that on the moon

Data : $G = 6.7 \times 10^{-11}$ N-m^2/kg^2,

M1=Mass of the Earth = 6×10^{24}kg.

M2=Mass of the moon = 6.7×10^{22}kg.

c) Find the magnetic field intensity $\bar{H}$ at a point P at a distance Z along the Z axis due to circular loop which carries a current of I amperes.

d) Prove that $\nabla.\bar{D} = \rho v$.

SECTION - II

Q4) Solve any two : **[16]**

a) The circular loop conductor lies in the z = 0 plane, has a radius of 0.1 meter and resistance of 5 ohm. Given $\bar{B} = 0.20 \sin 10^3 t\, \bar{a}_z$ (T), determine the current in the loop.

b) Discuss in detail Maxwell's equations for harmonically varying fields.

c) A plane wave traveling in air is normally incident on a material with $\varepsilon_r = 4$ and $\mu_r = 1$. Find the reflection and transmission coefficients.

Q5) Solve any two : **[16]**

a) Derive Helmholtz's equations for conducting media in plane wave propagation.

b) The electric field amplitude of a uniform plane wave propagating in the z direction in the free-space is 250V/m. If E x = E x and ω = 1.00Mrad/s, find :

i) The frequency; ii) The wavelength;

iii) The period iv) The phase shift constant and

v) The impedance

c) A lossless transmission line is 80cm long and operates at a frequency of 600 MHz. The line parameters are L = 0.25 μH/m and C = 100 pF/m. Find the characteristic impedance, the phase constant, and the phase velocity.

Q6) Solve any three : **[18]**

a) Comparison between circuit theory and field theory.

b) Infinite line

c) Single stub matching

d) Smith chart

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Total No. of Pages : 2

T.E. (Electronics Engg.) (Semester - V) (Revised) Examination, April - 2019

MICROCONTROLLERS

Sub. Code : 66281

Day and Date : Saturday, 27 - 04 - 2019 **Total Marks : 100**

Time : 02.30 p.m. to 05.30 p.m.

Instructions : 1) All questions are compulsory.
2) Assume suitable data if necessary.
3) Figures to the right indicate full marks.

SECTION - I

Q1) Answer Any 4 of the following. **[20]**

a) Draw and explain the format of TCON sfr of 8051.

b) Compare between 89c51 and 89c52 Microcontrollers.

c) Explain the PCON SFR with its format.

d) Explain the rotate instructions of 8051 with suitable example.

e) Draw port-0 internal structure and explain it briefly.

Q2) Answer Any Two of the following. **[16]**

a) Write ASM code to find the sum of 15 numbers stored in XRAM & keep answer in IRAM.

b) Explain the bit level Boolean instructions of 8051.

c) Explain the Timer/Counter mode -2 of 8051 with suitable diagram.

Q3) Answer Any Two of the following. **[14]**

a) Write ASM code to receive the block of data (5 characters) serially at 9600 baud using On- chip UART Port of 8051 and store it in IRAM address 40H onwards.(assume crystal frequency = 12 MHz.)

b) Draw and explain interfacing of a seven segment display to 8051.

c) Draw a hardware interface of stepper motor to 8051 and explain it in brief.

P.T.O.

SECTION - II

Q4) Answer Any 4 of the following. **[20]**

a) Describe embedded C data types.

b) What are the various RESET options available in PIC 16F877? Explain in brief.

c) Draw the interfacing of common cathode seven segment display to 8051.

d) Write embedded C code to add the contents of Port-0 & Port- 1.

e) What is the role of watch dog timer? List the SFRs associated to watch dog timer of PICI6F877.

Q5) Answer Any 2 of the following. **[16]**

a) Draw the interfacing of 4 * 4 Keypad to 8051 and explain how a key closure is detected.

b) Write assembly language program to add 10 bytes and send the result to Port-A using PIC 16F877 instructions.

c) Draw a block diagram of Timer-0 module of PIC16F877 and explain in brief.

Q6) Answer Any 2 of the following. **[14]**

a) Write assembly language program to swap the nibbles of a data present at PORT-B and send the result to PORT-C using PIC16F877 instructions.

b) Draw & explain the program memory map of PIC16F877.

c) Draw a block diagram of on-chip ADC of PICl6F877and explain it in brief

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Total No. of Pages : 3

T.E. (Electronics) (Part - II) (Semester - VI) Examination, May - 2019

Electronic System Design

Sub. Code : 66855

Day and Date : Thursday, 23 - 05 - 2019 **Total Marks : 100**

Time : 10.00 a.m. to 01.00 p.m.

Instructions :
1) **Draw neat circuit diagram where ever necessary,**
2) **Clearly specify assumptions if any.**
3) **Numbers to right indicate full marks**
4) **Write answers to bits in questions at one place and in sequence. Do not place answers randomly.**

SECTION - I

Q1) Answer the following : **[18]**

a) Explain various factors affecting reliability of equipment.

b) Explain with neat circuit diagram, how the SPDT relay (coil rating 5V, 30mA) can be connected to a CMOS logic output (CMOS IC is supplied by 10V Vdd)

c) List and explain the characteristics of an operational amplifier to be used as high frequency small signal amplifier.

Q2) Answer any two of the following : **[16]**

a) The output from a load cell changes at 20µ V/kg. The load cell delivers l2mV with no load on the cell. Design a zero and span (gain offset) convertor using an instrumentation amplifier that will output 0V dc when there is no load, and will change at 10m V/kg.

b) Design a signal conditioning circuit for RTD PT-100 to get output of 10mV/°C and 0 mV at 0°C, to detect temperature in the range of 0 to 50°C. Output voltage of signal conditioning circuit should be 0 to 0.5V corresponding to range of temp.

c) Design a grounded load I to V convertor that will convert 4 to 20mA current signal into a 0 to 5V ground referenced voltage signal.

P.T.O.

Q3) Answer any two of the following : **[16]**

a) Explain the I_2C protocol that uses 10 bit addressing. Explain Start and Stop conditions with waveforms, Explain various conditions under which master will terminate communication.

b) List and explain the factors responsible for selection of microcontroller used for electronic system.

c) Draw a detailed interface diagram to interface 4 no of seven segment LED display nodules to 8051 microcontroller using dynamic display interface. Use Common Anode displays modules, use Port 1 to interface segments 'a' to 'dp' and P2.0 to P2.3 lines to drive display modules.

SECTION - II

Q4) Solve any three :

a) With neat diagram discuss principle and working of Pulse oximeter. **[6]**

b) Discuss ECG signal characteristics from design perspective. **[6]**

c) How precautions in software can improve immunity against EMI interference. **[6]**

d) Discuss methods to reduce emission from microprocessor clock or ALE signal. **[6]**

Q5) Solve any two

a) What should be CMRR of differential input ECG amplifier if maximum common mode signal picked from 230 Vol AC mains is 1.5 volts (RMS), maximum Differential ECG signal is 2.5mv (RMS)and output of ECG amplifier is given to a 12 bit ADC with, ADC reference voltage of 4.096 Volts. **[8]**

b) Plan design and schematic diagram of blood glucose measurement to meet following specifications. **[8]**

i) Glucose measurement range: 20 mg/dl to 600 mg/dl (1 mmol/l to 33 mmol/l)

ii) Test strip sensing: To detect insertion of the test

iii) Provision to trigger microcontroller to detect blood sample on strip

iv) Starts recording the ADC readings, 1.5 seconds after the test sample is placed on the test strip and calculates the average

v) Calculates the glucose concentration using the regression equation (or Lookup table approach)

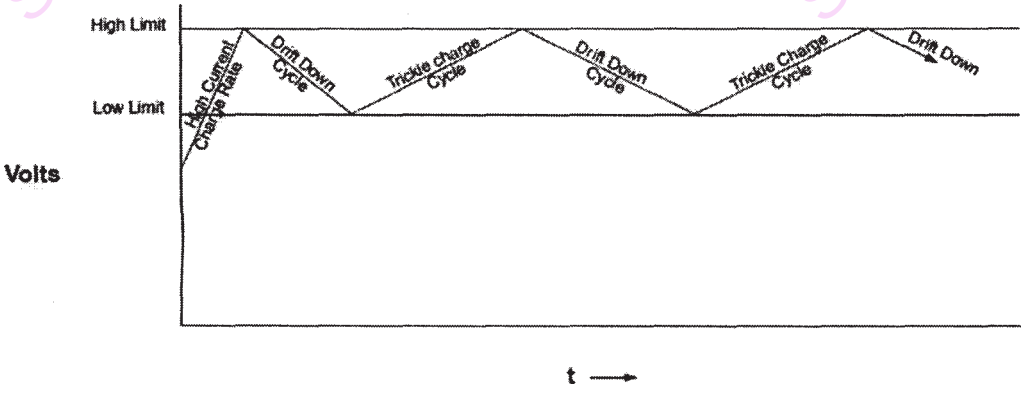
vi) Draw flowchart of firmware to be implemented on microcontroller of your choice

c) Plan design and schematic of infusion pump drug delivery system, discuss design. **[8]**

Q6) Solve any two

a) Design step up DC to DC converter with input 5 Volts DC and output 12 Volts DC with Output current not more than 500 ma and ripple not more than 100 mv. **[8]**

b) Plan and drawschematic of a Microcontroller based battery charger for lead acid battery of 12 volts 30 amp-hrs. The charger should follow following algorithm: Till battery voltage reaches 13.5, charge battery with constant current of 2 amps. If battery voltage crosses above 13.5 volts the current to battery should be cutoff, allowing the battery voltage to decay until it descends past the low limit (12.5V).A low current charge (150 mA) is then applied to againbring the battery voltage up past the high limiti.e 13.5 volts.The driftdown/trickle charge cycle repeats till battery removed from charger. Draw flowchart of program. Assume suitable data when needed. **[8]**



c) With suitabl circuit diagram and waveform explain working of Step down DC to DC converter. **[8]**

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T.E. (Electronics) (Semester - VI) (Revised) Examination, May - 2019
DIGITAL SIGNAL PROCESSING
Sub. Code : 66851

Day and Date : Monday, 13-05-2019 **Total Marks : 100**

Time : 10.00 a.m. to 1.00 p.m.

Instructions : 1) Figures to right indicate full marks.
2) Assume suitable data if required.

SECTION - I

Q1) Attempt any Two : **[18]**

a) Explain in detail Radix 2, DIF FFT Algorithm.

b) Compare Overlap Save method and Overlap add Method of Sectioned Convolution.

c) State and Prove any two properties of DFT.

Q2) Attempt any Two : **[16]**

a) Find the inverse DFT of X(k) = {1, 2, 3, 4}.

b) Explain various applications of Wavelet Transform.

c) What are the advantages and disadvantages of FIR Filters? What is the necessary and sufficient condition for the linear phase characteristic of an FIR Filter?

Q3) Attempt any Two : **[16]**

a) Design a FIR high pass filter with cutoff frequency of 1.5 KHz and sampling frequency of 5KHz with 7 samples using Fourier Series Method. Determine the frequency response.

b) Compare various types of window functions used in Design of FIR Filters.

c) Explain in detail step by design of FIR filter using Kaiser Window.

P.T.O.

SECTION - II

Q4) Attempt any Two : **[18]**

a) Explain in detail bilinear Transformation Method.

b) Determine H(z) using the impulse invariant Technique for the analog system function

$$H(S)=\frac{1}{(s+0.5)(s^2+0.5s+2)}.$$

c) Explain in detail various steps in design of digital Butterworth IIR Low pass Filter.

Q5) Attempt any Two : **[16]**

a) Explain in detail Cascade form and Parallel form of Realization of IIR Systems.

b) Explain various addressing modes of TMS320C67XX Processor.

c) Write a note on 'Effect of Finite Word Length'.

Q6) Attempt any Two : **[16]**

a) Explain the need of Multirate Digital Signal Processing. Give some Examples of Multirate Systems.

b) Explain Decimation and Interpolation Process with example.

c) Explain in detail two Stage Interpolator.

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Total No. of Pages : 2

T.E. (Electronics) (Semester - V) Examination, May - 2019

DIGITAL COMMUNICATION (Revised)

Sub. Code : 66284

Day and Date : Wednesday, 08 - 05 - 2019 **Total Marks : 100**

Time : 02.30 p.m. to 05.30 p.m.

Instructions : **1)** **All questions are compulsory.**

2) **Figures to the right indicate full marks.**

SECTION - I

Q1) Attempt any three: **[18]**

a) What is CDF? Explain its properties in brief with proof.

b) Explain joint distribution function for discrete and continuous signal.

c) Write note on "Gaussian distribution'

d) What is the need of frame synchronization? Explain.

Q2) Attempt any two: **[16]**

a) Derive an expression for signal to noise ratio in PCM based system.

b) An audio signal has spectral component present in the range of 300 Hz to 3300 Hz. A PCM signal is generated by sampling frequency of 8 KHz. The minimum value of signal to noise ratio is 30 dB. Calculate:

i) The minimum level of quantization levels Q and number of binary digits per word, N.

ii) Signaling rate.

iii) Minimum transmission Bandwidth.

c) Draw and explain with block diagram Linear Delta modulation.

P.T.O.

Q3) Attempt any two: **[16]**

a) Explain the M^{th} power loop method for carrier recovery.

b) What is quantization? Explain in detail Uniform quantization.

c) Represent the data 10101001 using the following data formats with the help of waveform:

i) Biphase -M

ii) Bipolar NRZ

iii) Uni-polar RZ

iv) Split phase Manchester format

SECTION - II

Q4) Attempt any two: **[18]**

a) What is the ISI? Explain its cause and remedy to reduce.

b) Discuss the properties and application of matched filter.

c) What is the necessity of equalization in digital transmission? What is adaptive modulation?

Q5) Attempt any two: **[16]**

a) Explain the QPSK modulation scheme with suitable transmitter and receiver diagram.

b) Draw and explain Duo-binary baseband PAM system.

c) Explain transmitter and receiver of FSK with neat diagram and waveform.

Q6) Attempt any two: **[16]**

a) Explain eye pattern with suitable diagram.

b) Explain Direct sequence spread spectrum (DSSP) and state its advantages.

c) With help of neat diagram explain Frequency hopping spread spectrum.

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Total No. of Pages : 2

T.E. (Electronics Engineering) (Semester - VI) (Revised) Examination, May - 2019

COMPUTER ARCHITECTURE & OPERATING SYSTEMS

Sub. Code : 66854

Day and Date : Tuesday, 21 - 05 - 2019 **Total Marks : 100**

Time : 10.00 a.m. to 01.00 p.m.

Instructions : **1)** **All questions are compulsory.**

2) **Assume suitable data if necessary.**

3) **Figures to the right indicate full marks.**

SECTION - I

Q1) Answer Any Two of the following : **[16]**

a) Explain two's complement multiplier.

b) Describe Booth's algorithm for multiplication. State its advantages.

c) Draw a flowchart of the accumulator based CPU.

Q2) Answer Any Two of the following : **[16]**

a) Explain the design of control unit organization of typical micro-programmed controller.

b) Draw and explain IEEE-754 Floating point data format.

c) Draw and explain floating point pipelined adder.

Q3) Answer Any Three of the following : **[18]**

a) What is meant by system software? List the various types with its use.

b) Define the terms

i) I/O Manager

ii) Multitasking

iii) Spooling

c) Explain combinational array multiplier.

d) Explain Robertson's multiplication algorithm.

P.T.O.

SECTION - II

Q4) Answer Any Two of the following : **[2 × 8 = 16]**

a) What is CPU starvation? Explain any method to avoid it.

b) Explain Process control block in detail with neat diagram.

c) What is a reentrant code? Explain its effect on shared memory concept.

Q5) Answer Any Two of the following : **[2 × 8 = 16]**

a) Explain memory fragmentation in detail. Explain two types of fragmentation.

b) Explain demand paging in detail with neat diagram.

c) Explain process synchronization and resource synchronization with reference to semaphores.

Q6) Write short notes on any three of the following : **[3 × 6 = 18]**

a) Race Condition

b) Deadlock

c) Page replacement methods

d) Process Vs Threads

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T.E. (M) (Semester - V) Examination, April - 2019

CONTROL ENGINEERING

Sub. Code: 66241

Day and Date : Thursday, 25 - 04 - 2019 **Total Marks : 100**

Time : 2.30 p.m. to 5.30 p.m.

Instructions : **1)** **All questions are compulsory.**

2) **Assume suitable data if required and mention it clearly.**

Q1) a) For the mechanical system shown in Fig. 1a construct grounded chair representation and find equation relating *f* to *x* and *x* to *y* **[6]**

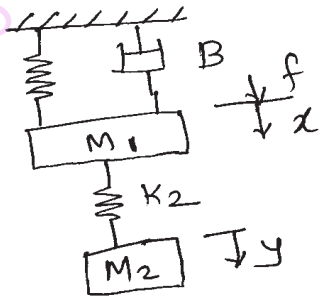
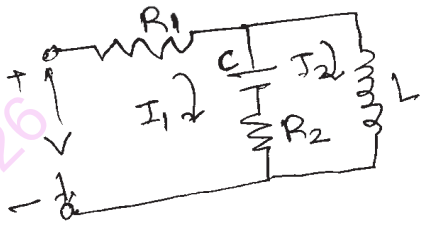


fig 1 a

b) Explain mathematical model of hydraulic system. **[6]**

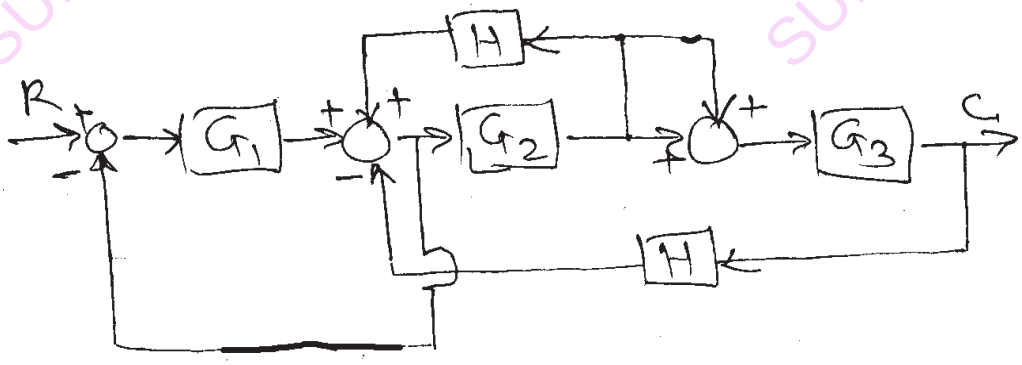
c) Construct direct and Inverse analog for Electrical circuit shown in fig. Find mechanical circuit with equations. **[6]**



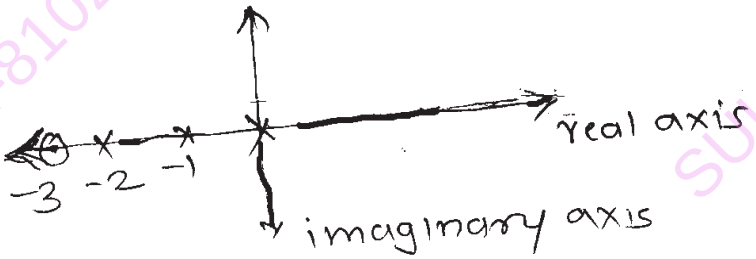
P.T.O.

Q2) a) What do you mean by linearization of non-linear function. Explain geometric, interpretation of error in the measurement of area of a rectangle having width W and length L. **[8]**

b) Find the transfer function for the block diagram shown in fig. **[8]**



Q3) a) Pole zero configuration of the overall transfer function is shown in fig. Determine its response for unit step input. **[8]**



b) The step response of a second order control, control system is shown in figure. Determine closed loop transfer function of the system. **[8]**

Q4) a) Using Rootn stability criterion. Determine stability of system having its open loop transfer function has poles at s = 0, s = – 1, s = – 3 and zero at s = – 5 take gain k = 10. **[8]**

b) Sketch root locus for $G(s)\cdot H(s)=\dfrac{k(s+2)}{(s+1+j\sqrt{3})(s+1-j\sqrt{3})}$. **[10]**

Q5) a) Draw bode plot for transfer function $G(s)=\dfrac{1000}{s(1+0.1s)(1+0.001s)}$.

Determine gain margin and phase margin. **[10]**

b) Calculate break in point and angle of departure for control system given by characteristic equation $s^2+2s+3+k(s+2)=0$. **[6]**

Q6) a) Determine state space representation and computer diagram using series programming $y(t)=\dfrac{2(D+5)}{(D+2)(D+3)(D+4)}f(t)$. **[8]**

b) Determine state space representation and computer diagram using general programming $y(t)=\dfrac{D+3}{D^3+9D^2+24D+20}f(t)$. **[8]**

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Total No. of Pages : 2

T.E. (Electronics) (Semester - V) (Pre-Revised)
Examination, May - 2019
DIGITAL SYSTEM DESIGN (Old)
Sub. Code : 45591

Day and Date : Friday, 10 - 05 - 2019 **Total Marks : 100**

Time : 02.30 p.m. to 06.30 p.m.

Instructions : **1)** **All questions are compulsory.**
2) **Figures to the right indicate full marks.**
3) **Assume suitable data if required.**

SECTION - I

Q1) Attempt any THREE : **[3 × 6 = 18]**

a) Write syntax for following VHDL statements
   i) with_select
   ii) Process
   iii) Case

b) Write a VHDL code for 1-bit magnitude comparator.

c) Write a note on data types available in VHDL.

d) Write a note on “Signal” & “Variable”.

Q2) Attempt any TWO : **[2 × 8 = 16]**

a) Write a note on “Clock Skew” & “Clock Jitter”.

b) Draw and explain VLSI design flow.

c) Write a note on operators available in VHDL.

Q3) Attempt any TWO : **[2 × 8 = 16]**

a) Write a VHDL Code for BCD up-down counter in behavioral modeling.

b) Write a VHDL code for D-FF using.
   i) Synchronous reset
   ii) Asynchronous reset

c) Explain Mealy machine & Moore machine with suitable examples.

P.T.O.

SECTION - II

Q4) Attempt any THREE : **[3 × 6 = 18]**

a) Write a note array and data attributes.

b) What are the different phases of simulation cycle?

c) Draw and explain function block of XC9572 CPLD.

d) With neat labeled diagram explain BIST testing technique.

Q5) Attempt any TWO : **[2 × 8 = 16]**

a) Explain the working of event driven simulators with the help of flowchart.

b) Draw and explain architecture of XC9572 CPLD.

c) Draw and explain s_a_0 & s_a_1 model of testing.

Q6) Attempt any TWO : **[2 × 8 = 16]**

a) Draw and explain CLB of xc2s30 Spartan-II FPGA.

b) Explain Inertial and Transport delays with appropriate diagrams.

c) Draw and explain designing of Datapath for EC-2 processor.