**D.Y. PATIL COLLEGE OF ENGINEERING & TECHNOLOGY**

**22SYAIML203303**

**Q. Paper Code:**

**KASABA BAWADA KOLHAPUR-416006**

**(An Autonomous Institute)**

**S. Y. B. Tech CSE-AIML(Semester-III)**

**END SEMESTER EXAMINATION, OCT./NOV. - 2021-22**

COURSE NAME: Computer Architecture and Microprocessors, COURSE CODE:201AIMLL203

Seat No :

**Day and Date: Tuesday, 08/02/2022**

**Time: 10.00am to 11.00am Max. Marks- 50**

**OBJECTIVE**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Unit 1 |  | 3questionsof2markseach | 6marks | 20marks | 40% |
| Unit 2 |  | 3questionsof2markseach | 6marks |
| Unit 3 |  | 4questionsof2markseach | 8marks |
| Unit 4 |  | 5questionsof2markseach | 10marks | 30marks | 60% |
| Unit 5 |  | 5questionsof2markseach | 10marks |
| Unit 6 |  | 5questionsof2markseach | 10marks |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | | |  | Correct  Option |
| Q. 1) | Which microprocessor has multiplexed data and address lines? | | A |
| A) 8086 | B) 80286 |
| C) 80386 | D) Pentium |
| Q. 2) | Which is not part of the execution unit (EU)in 8086? | | C |
| A)Flags | B) Arithmetic logic unit (ALU) |
| C)Clock | D) General registers |
| Q.3) | Register RAX in programming model of 80X86 family is of size | | D |
| A) 8bit | B) 16 bit |
| C) 32 bit | D) 64 bits |
| Q. 4) | Whenever the data is found in the cache memory it is called as \_\_\_\_\_\_\_\_\_ | | B |
| A) MISS | B) HIT |
| C) FOUND | D) ERROR |
| Q. 5) | In DMA transfers, the required signals and addresses are given by the \_\_\_\_\_\_\_\_\_\_ | | A |
| A ) DMA controllers | B) ) Processor |
| C) The program itself | D) Device drivers |
| Q. 6) | Interrupt driven I/O is more efficient than | | D |
| A) I/O Module | B) CPU |
| C) I/O device | D) Programmed I/O |
| Q. 7) | What is computer organization? | | A |
| A)structure and behavior of a computer system as observed by the user | B)structure of a computer system as observed by the developer |
| C) structure and behavior of a computer system as observed by the developer | D) All of the mentioned |
| Q. 8) | To increase the speed of memory access in pipelining, we make use of \_\_\_\_\_\_\_ | | C |
| A) Special memory locations | B) Special purpose registers |
| C) Cache | D) Buffers |
| Q. 9) | A type of parallelism that uses micro architectural techniques. | |  |
| A)instructional | B)bit level  A |
| C)Bit based | D)increasing |
| Q. 10) | The pipelining process is also called as \_\_\_\_\_\_ | |  |  |
| A) Superscalar operation | B) Assembly line operation  B |
| C) Von Neumann cycle | D) None of the mentioned |
| Q. 11) | Which of the following is not a machine control instruction? | | B |
| A) HLT | B) CLC |
| C) LOCK | D) ESC |
| Q.12) | ALE pin of 8085 microprocessor is used to | | D |
| A)latch the output of an I/O instruction into an external latch | B) deactivate the chip-select signal from memory device |
| C) find the interrupt enable status of the TRAP interrupt | D) latch the 8-bit of address lines AD0-AD7 into an external latch |
| Q. 13) | What is the order decided by a processor or the CPU of a controller to execute an instruction? | | B |
| A) fetch,execute,decode | C)decode,fetch,execute |
| B) fetch,decode,execute | D) execute,fetch,decode |
| Q. 14) | Addressing mode of instruction MOV B,M is | | A |
| A) Indirect Addressing mode | B) Register addressing mode |
| C)Direct addressing mode | D) Immediate addressing mode |
| Q. 15) | If A=10000001 & CY=0 after execution of RAR instruction status of A & CY is | | C |
| A) A=01000000 CY=0 | B) A=00000011 CY=0 |
| C) A=01000000 CY=1 | D) A=00100000 Cy= 1 |
| Q. 16) | On power up, the 8051 uses which RAM locations for register R0- R7 | | B |
| A) 00-2F | B) 00-07 |
| C) 00-7F | D) 00-0F |
| Q. 17) | How are the bits of the register PSW affected if we select Bank2 of 8051? | | D |
| A) PSW.5=0 and PSW.4=1 | B) PSW.2=0 and PSW.3=1 |
| C) PSW.3=1 and PSW.4=1 | D) PSW.3=0 and PSW.4=1 |
| Q. 18) | How many bytes of bit addressable memory is present in 8051 based microcontrollers? | | A |
| A) 16 bytes | B) 8 bytes |
| C) 32 bytes | D) 128 bytes |
| Q. 19) | The instructions that change the sequence of execution are | | C |
| A) conditional instructions | B) logical instructions |
| C) control transfer instructions | D) data transfer instructions |
| Q. 20) | The internal RAM memory of the 8051 is: | | B |
| |  | | --- | | A) 32 bytes | | |  | | --- | | B) 128 bytes | |
| C) 64 bytes | D) 256 bytes |
| Q.21) | The instructions that pass through the fetch, decode and execution stages sequentially is known as | | C |
| |  | | --- | |  | | A) sequential instruction |  | |  |  | |  |  | | B)sequence of fetch, decode and execution |
| C) linear instruction sequencing | D) non-linear instruction sequencing |
| Q. 22) | The unit that is used to implement the multiple branch prediction in Pentium-Pro is | | A |
| A) branch target buffer | B) bus interface unit |
| C) control unit | D) branch instruction register |
| Q. 23) | The unit that accepts the sequence of instructions from the instruction cache as input is | | C |
| A) retire unit | B) dispatch-execute unit |
| C) fetch-decode unit | D) none |
| Q. 24) | Which of the following is not an independent engine of Pentium-Pro? | | D |
| A) fetch-decode unit | B) dispatch-execute unit |
| C)retire unit | D)control-execute unit |
| Q. 25) | Because of Pentium’s superscalar architecture, the number of instructions that are executed per clock cycle is | | C |
| A) One | B) Three |
| C)Two | D) Four |

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**S. Y. B.Tech./B.Arch (Semester-III)**

**END SEMESTER EXAMINATION, OCT/NOV- 2021-22**

COURSE NAME:CSE ( Artificial Intelligence and Machine Learning) COURSE CODE: 201AIMLL203

Seat No :

**Day and Date: Tuesday, 08/02/2022**

**Time: 11.00am to12.30pm Max. Marks- 50**

***Instructions:***

1. *All Questionsare compulsory.*
2. *Figure to the right indicate full marks.*
3. *Give suitable general Instructions*
4. *Any other Course Specific Instructions.*

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **BTL** | **CO** | **Q. No.** |  | **Marks** |
|  |  | **Q.1)** | **Attempt the following** | **20** |
|  | **CO1** | **a** | Explain evolution of intel X86 architecture | **7** |
|  | **CO2** | **b** | Explain Pentium 4 and Power PC Cache Organization | **7** |
|  | **CO3** | **c** | Explain DMA concept in detail | **6** |
|  |  | **Q.2)** | **Attempt the following** |  |
|  | CO4  CO5 | a | I) Explain difference between Microprocessor & Microcontroller OR  II)Internal structure of Pentium pro | **7** |
|  | CO4 | b | I)Explain data transfer group of instructions in 8085with example  OR  II)Explain instruction execution in 8085 | **8** |
|  |  | **Q.3)** | **Attempt the following** |  |
|  | CO5  CO4 | a) | I)Explain memory management in Pentium processor  OR  II)Explain 8051 microcontroller architecture | **7** |
|  | CO4  CO5 | b) | I) Explain addressing modes in 8085 OR  II) Explain special Pentium registers | **8** |